chapter 4 hw

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4.8 , 4.12 , 4.13.2 , 4.13.4

4.8

1. 250ps, 350ps

2. 1250ps, 1750ps

3. split ID , the new cycle time 300ps

4. 35%

5. 65%

6. execution time is 3.57 times the pipelined version Multi-cycle : clock cycle is 350ps, execution time is 4.2 times the pipelined version

4.12

1. 46%

2. 17%

3. MEM/WB

4. 1.54

5 0.72

6. MEM/WB

4.13.2

add r5 r2 r1

lw r2 0(r2)

nop

nop

lw r3 4(r5)

nop

nop

nop

or r3 r5 r3

nop

nop

nop

sw r3 0(r5)

no performance

4.13.4

ForwardA = ForwardB = 00